EFFECTS OF ARC-BACK FAULT IN VSD SYSTEMS AND HOW TO PROTECT AGAINST THEM

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Abstract – VSD related arc-back faults have been discussed in technical forums without detailed explanation. However, the consequences of this fault mechanism is generally unknown by the engineers working in the industry. Scientific literature generally tend to ignore it. The phenomena is described in IEEE 551 but only for a theoretically ideal system without losses, saturation of the transformer or other overall system components.

This technical paper aims to explain the theoretical background of arc-back and, by simulations, to demonstrate the actual performance of the real system where the stresses are reduced by system resistances. This type of single diode failure causes high thermal and dynamic stresses on the drive input transformers being known to be behind transformers failures with production loss and long recovery times. This paper also explains the principles how to protect the VSD drive transformer against this detrimental mode of component failure by rectifier monitoring.

The aim of the authors is to get this phenomena know and understood. It shall also be noticed in international and national standards and specifications of VSD drives. The overall target is to improve the reliability of these important industrial work horses by increasing the understanding of the importance of the correct specifications of drive transformers and drive protection.

Index terms **–** Transformer, Arc-back, Variable Speed Drive System, Diode, Semiconductor failure, Protection, Thermal fault, Short-Circuit.

I. INTRODUCTION

The term ‘arc-back’ means that a semiconductor component has a breakdown so that it conducts also during the reverse voltage. Other names for arc-back are ‘reverse breakdown’ and ‘avalanche breakdown’. It is presented in IEEE 551 ([3], pp. 187-196) with examples. *“Analysis of converter design and operating experience shows that arc-back or failure of semiconducting rectifiers are the most common faults of converter systems. The calculation of arc-back currents is, therefore, one of the important concerns in the theory and application of converter systems.”* [[3], p.187].

Back in the history, the phenomena has been known already at least in the 40’s when mercury-arc power rectifiers were used since the early twenties [9, 10, 11, 12]. Thus, the name ‘arc-back’ is inherited from the past components but it is still used with modern semiconductors.

Previously, this fault type was practically a non-existing problem, since rectifying bridges were typically equipped with high-speed fuses to disconnect faulted semiconductors. The modern VSD drives are typically equipped with fuseless rectifying bridges, thus bringing arc-back fault back into the spotlight.

A short-circuit directly at the terminals of a diode rectifier transformer is probable. Thus, either the transformer has to be designed to withstand the short-circuit forces and thermal stresses, or the protection of the transformer against semiconductor failure has to be quick and reliable enough.

Arc-back faults related to variable speed drives (VSD) have been discussed in PCIC Europe Conference [1] and in IEEE Industry Applications Magazine [2] without going into detailed explanation. However, the consequences of this fault mechanism is generally unknown by the engineers working in the industry. Also handbooks, standards and educational material of power electronics generally tend to ignore it. The phenomena is described in IEEE 551 [3] but only for a theoretically ideal system without losses, saturation of the transformer or other overall system components.

The practice has shown that the typical IEC and IEEE standards short-circuit definitions [4, 5, 6] are not enough; but a diode fault is more demanding for a transformer than a three-phase short-circuit fault. The base of this study is in the standard IEEE 551-2006 [3] but in addition, further investigations are done. In IEC standards, the phenomena is not yet mentioned (year 2018).

The theoretical maximum current peak in arc-back fault is three times the three-phase short-circuit continuous fault current peak value [3]. The dc-component in an arc-back does not attenuate to zero similarly as it does in a three-phase short-circuit. The thermal stress for a transformer winding is thus higher in an arc-back fault. Also the frequency of the force oscillation is different in the faults.

This cooperative study between the organizations of the authors has been initiated, because of thermal damage in a transformer winding which could not be explained by the duration of the fault current as the actual tripping data from the breaker was available. Also in other publications the topic has been emphasized, for example in [2] and [13].

Typically in a VSD system, there are multiple secondaries in the transformer. Thus it is difficult to monitor the failure currents in the transformer primary side. The protection problems as well some protection options are discussed, for example in [1]. One protection possibility is to directly short-circuit the drive dc-link. This way, the transformer will suffer three-phase short-circuit, but the protection relay operates. Typically drive specifications require that the network side main circuit breaker has to operate in less than 100 ms.

From the transformer withstandability point of view, the best option to protect the transformer is to design it to withstand the whole current. This requires that the short-circuit duration is feasible and detectable. In this document, some advanced design aspects are introduced in order to help the designer to dimension the transformer.

II. THEORY

A. Normal Three-Phase Short-Circuit

In a normal three-phase short-circuit condition, the symmetrical short-circuit current remains but the dc-component is typically damped after 1-2 cycles. System impedances affect the damping time constant. Typically the withstandability verifications for a transformer are made as three-phase short-circuit and one-phase earth fault cases, as yielding the highest short-circuit currents and stresses. Highest current peak gives the highest dynamic forces and stresses, and highest RMS value gives the thermal stresses. This process is documented in IEC [5] and IEEE [7].

In a normal three-phase short-circuit, the amplitude of the first peak of the current after the fault is calculated with the aid of peak factor *k* and symmetrical current I_k (1).

$$\hat{\imath}_{firstpeak} = \sqrt{2} \cdot I_k \cdot k \qquad (1)$$

These √2·*k* factors depend on the ratio *X/R* and are determined in [5] and [7]. The asymmetric factor *k* describes the relation between the dynamic and symmetrical short-circuit currents.

B. Theoretical Arc-Back

Equation (2) is same as (8.30) in [3]. It describes the non-damped peak of the current feeding the fault point in a diode converter system in a diode failure.

$$I_{psc} = 3I_m \qquad (2)$$

where I_m is the peak of the symmetrical short-circuit phase-current in a three-phase short-circuit at the ac-input terminals of the converter [3]. In other words, the arc-back maximum current peak is three times larger than the peak of the phase-current at a three-phase short-circuit fault at continuous mode.

C. Comparison of the Fault Types

By comparing the highest current peaks of a normal three-phase short-circuit and an arc-back, the relation between the arc-back peak current (peak) and symmetric short-circuit current (RMS) is theoretically 3√2.

The factor “3” (2) is the theoretic maximum and applies for a system without resistances, and thus these factors are maximum values. In the following chapters, also factors for a real system are presented. Like the three-phase short-circuit values depend on the *X/R* value, also arc-back values depend on it.

III. SIMULATIONS

The simulations were implemented in PSCAD v. 4.6.2. In the simulations a 12-pulse rectifying circuit was implemented with a saturating transformer model [8]. The main parameters of the network were following:

- Supply network, 10 kV, Z_k = 0,4 Ω, angle 80°
- Transformer (YNynd)
  - S_N = 3306 kVA
  - U_Y = 1920 V
  - U_D = 1920 V
  - R_k varies between simulation runs
  - X_k varies between simulation runs

In the model faults were implemented in y-winding. For all runs, optimization of fault time were performed, with the goal of maximizing fault currents. All rectifying bridge diode faults were implemented in phase A of the y-winding. All three-phase faults were implemented in the middle point of the y-winding rectifying bridge.

The overall model of the system is described in Fig. 1. In the simulations the pulse number of the rectifying bridge did not seem to have significant effect. Thus, this paper presents only cases with 12-pulse rectifying bridge.

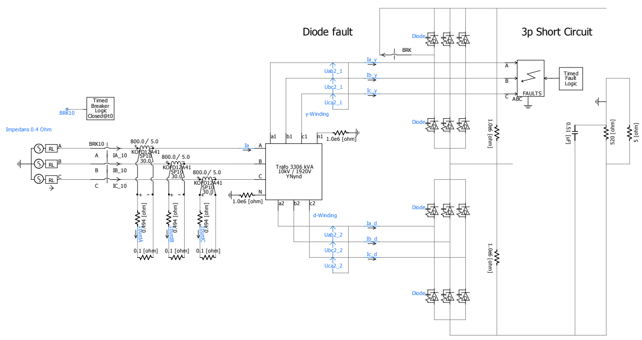

Fig. 1 12 pulse rectifying circuit

The model operation was first tested in as lossless case as it was possible to implement. Arc-back fault currents in lossless case are shown in Fig. 2 and three-phase fault in Fig. 3. From these figures the arc-back fault factor was calculated, which is described as a ratio between the absolute maximum peak current of the faulty diode phase and continuous three-phase fault current peak value (3).

$$R_{Arcback} = \left| \frac{\hat{I}_{DiodeFault,AbsMax}}{\hat{I}_{3PhaseFault,Continious}} \right| \qquad (3)$$

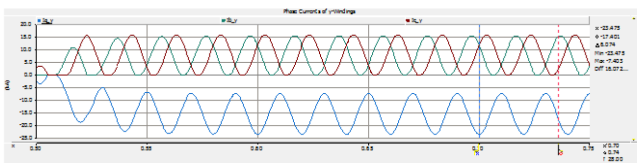

Fig. 2 Arc-back fault, lossless case

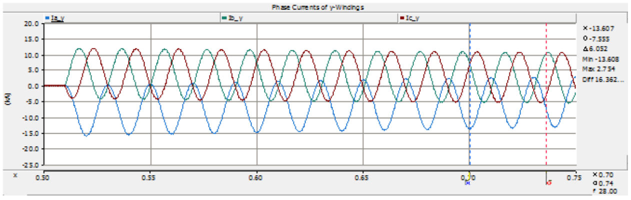

Fig. 3 Three-phase short-circuit, lossless case

The arc-back fault factor was 2.96, when theoretical maximum is 3 and there were some losses in the system. Thus, the model was good enough to proceed.

For the total *X/R* ratio, the grid and transformer ratios have been taken into account. The system was simulated with various *X/R* ratios of the system. As an example, here are the results for *X/R* total system ratio of 9.213, there the arc-back fault factor was only 2.01. The arc-back fault currents on transformer secondary side are shown in Fig. 4 and three-phase short-circuit currents are shown in Fig. 5. The saturating lossy transformer causes the fault current "slowly" to increase to maximum value and then decrease to continuous levels. In the arc-back fault the DC-component of the currents causes this phenomenon, since the fundamental stays quite stable during the fault, which can be seen from Fig. 7.

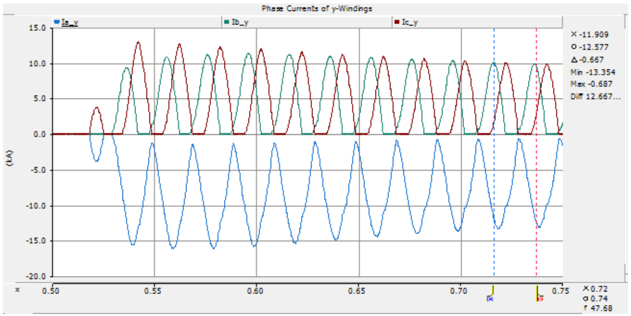

Fig. 4 Arc-back fault currents, actual transformer, system X/R 9.213.

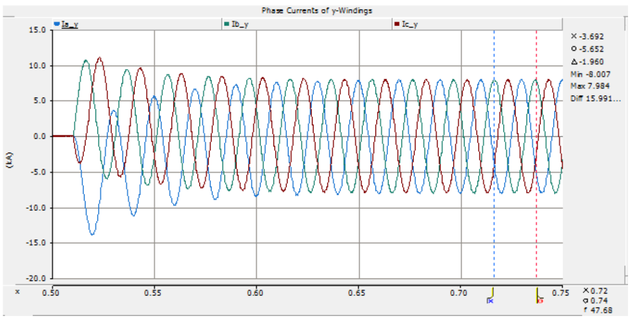

Fig. 5 Three-phase short-circuit currents, actual transformer, system X/R 9.213.

The system across realistic *X/R* ratios were simulated and based on these, there is a simple logarithmic model for arc-back fault factor, which is shown in Fig. 6. Based on Fig. 6, arc-back fault factor maximum is about 2.5 for realistic cases. For the theoretically ideal case the maximum is 3.0 as discussed above [3].

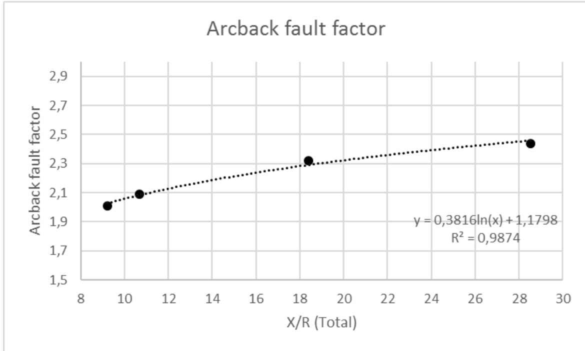

Fig. 6 Arc-back fault factor as a function of transformer *X/R*.

In Fig. 7, there are total RMS current, 50 Hz RMS current and the DC component current for low voltage windings in the diode failure in a realistic model and, and in Fig. 8, the respective curves for the three-phase short-circuit. In these example figures, the system X/R is 9.213.

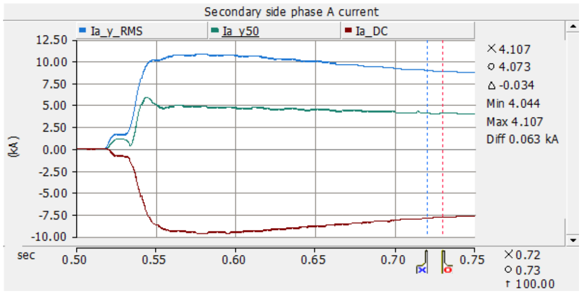

Fig. 7 Low voltage side RMS, 50 Hz RMS and DC currents (phase a) in a diode failure in real model (saturable with losses, total X/R=9.213).

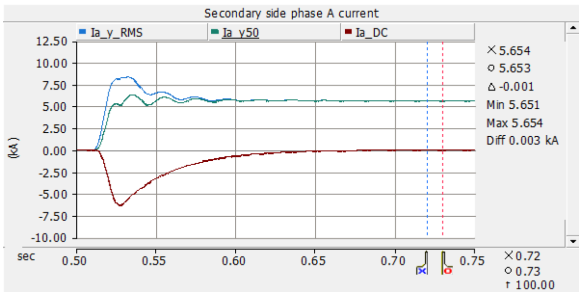

Fig. 8 Low voltage side RMS, 50 Hz RMS and DC currents (phase a) in a three-phase short-circuit in real model (saturable with losses, total X/R=9.213).

When comparing these figures (Fig. 7 and Fig. 8), it is clear that the DC component is higher in arc-back and practically it does not attenuate. Another thing, which is remarkable, is that the highest peak in an arc-back, is reached after some cycles after fault; whereas in three-phase short-circuit it occurs at the first half period. One possible reason for this might be the energy storage feature of capacitors in the intermediate circuit. This depends on the fault instant – what is the reverse voltage at the other side of the diode, what is the direction of the current – from/to the energy storage. The broken diode can affect the current not to rise earlier. Also, saturation of the transformer core could be another reason for decaying.

IV. ARC-BACK VALUES DEPENDING ON *X/R* RATIO

In the three-phase short-circuit, the *X/R* relation affects the severity of the dynamic stress. Also in the diode failure, *X/R* has effect. When *X/R* ratio decreases, the fault current damping is more effective. When *X/R* ratio increases it gets closer to the ideal, lossless case. In this chapter, the factors are presented. In the figures, the grid effect on X/R has been taken into account.

Firstly, the ratio of the arc-back largest peak to the three-phase continuous mode fault current RMS value I_k is to be considered in order to calculate the dynamic force and caused stresses. The highest current peak is used to calculate the dynamic stresses on the transformer. The dynamic peak factor *D* (arc-back highest current peak in comparison to three-phase short-circuit continuous mode RMS current I_k) dependency on *X/R* relation is illustrated in Fig. 9 and it follows (5).

$$D = -0.0015\left(\frac{X}{R}\right)^2 + 0.0891\frac{X}{R} + 2.1656 \qquad (5)$$

For theoretically ideal arc-back system: D= $3\sqrt{2} \approx 4.243$.

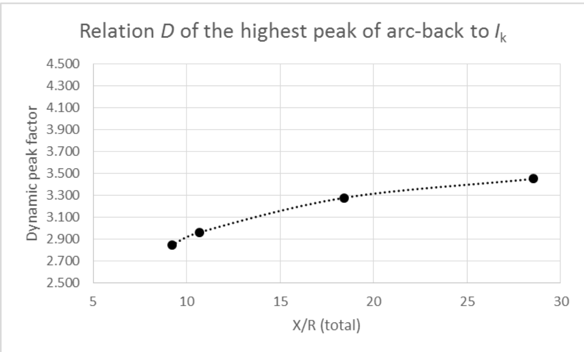

Fig. 9 Dynamic peak factor *D* dependency of *X/R* ratio according to simulation results.

Secondly, the relation of the continuous arc-back RMS current value and the three-phase continuous mode RMS current value I_k is to be considered in order to calculate the thermal stresses in the low voltage windings. For the continuous mode factors *C,* the dependency of *X/R* is in the following curve (Fig. 10) and (6) applies.

$$C = 0.6384\ln\frac{X}{R} + 0.1748 \qquad (6)$$

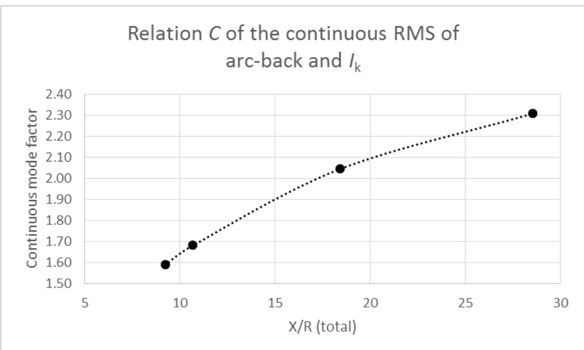

Fig. 10 Relation *C* of the continuous mode RMS values of both arc-back and three-phase short-circuit currents as a function of *X/R.*

Furthermore, the relation *A* of the dynamic and thermal arc-back currents is in Fig. 11. The relation is also in the following (7). These factors *A* are similar to the peak factor (I_{dyn}/I_{sym}) of three-phase short-circuit calculation procedure but for arc-back currents, not for three-phase currents.

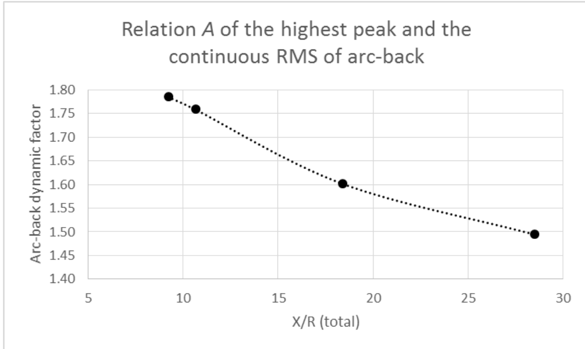

Fig. 11 Arc-back dynamic peak in relation to arc-back continuous RMS value as a function of *X/R*, i.e. arc-back dynamic factor *A*.

$$A = 0.0005\left(\frac{X}{R}\right)^2 - 0.0338\frac{X}{R} + 2.0586 \qquad (7)$$

The limited amount of points affects the equations, thus these equations (5, 6 and 7) are approximations and apply only for the total system values *X/R*= 9.21 … 28.53. The theoretical maximum has to be taken into account separately in case of interest.

The theoretical value 3.0 from literature [3] is the peak relation value and it is applicable for an ideal circuit. In practice applying the theoretical value directly increases the costs of a transformer unnecessarily. Obviously, a value based on real transformer *X/R* is smaller and correct for a transformer design. The practical peak relation value varies according to the *X/R* relation, and also the RMS values shall be taken into account. Furthermore, in the design process, it shall be noted that the DC-component is large and the wave form is non-sinusoidal having high harmonic content.

V. EFFECTS ON TRANSFORMERS

In some cases, the first indication about the problem is gas relay alarm. If this last warning is not taken seriously and the transformer is then switched on without checking the diodes, the transformer can fail. Temporary hot insulation can be acceptable, with shorter lifetime, but switching impulse and repeated arc-back short-circuit will break the transformer finally through the insulations.

As a comparison of a three-phase short-circuit to the arc-back short-circuit: the dc-component in an arc-back does not attenuate to zero as it does in a three-phase short-circuit. The thermal stress for a transformer winding is thus higher in an arc-back fault. In some cases, thermal damage in a transformer winding cannot be explained by the duration of the fault current. The explanation to the thermal damages can be arc-back according to the simulation results showed above.

In a pure three-phase short-circuit the harmonic content can be more or less negligible according to theory. On the contrary, in an arc-back, two of the phases have only every second half-waves, which increases the harmonic content significantly.

Furthermore, in an arc-back, the transformer core gets saturated. Once saturated, there is also magnetization current flowing in the high voltage winding. Only the air core impedance (impedance for saturated) and grid are limiting the magnetization current at the saturation mode. According to the simulations, phase DC current components are not damped in case the model is non-saturable (i.e. theoretical), but with more realistic saturable transformer model the phase DC currents attenuate. Furthermore, in comparison to the saturable model, the saturation increases the THD over 100 % occasionally in the phase having the largest current, in the other two phases THD is increased by 7…9.5% or 27..31% in one simulation example.

In the non-saturable case, the first peak is nearly as large as the second peak, whereas in the saturable cases the first peak is always lower than the second. Furthermore, when *X/R* relation increases, the highest low voltage current peak increases because it gets closer to the ideal, lossless case. The highest current peak is used for the dynamic stresses.

Due to higher currents, also the stressing forces are higher. Forces are proportional to the square of the currents, the peak forces are respectively proportional to the peak currents. Also, different to AC short-circuits, where the force oscillates at a frequency twice the fundamental frequency (100 Hz at 50 Hz grid), in arc-back faults, the force oscillates with the fundamental frequency (50 Hz at 50 Hz grid).

VI. PROTECTING AGAINST ARC-BACK FAULT

As discussed during a diode failure the stresses in the transformer are high and it is imperative that the drive system acts to minimize the stresses in the circuit and thus prevent system damage. This action can be separated into two constituent parts; a reliable detection mechanism and a fast mechanism to eliminate the asymmetric current and the associated stresses on the transformer.

It is possible to assign both tasks to medium voltage fuses installed in the circuit between the rectifier diodes and the transformer. For this solution to work reliably, the selection of the fuse becomes critical to minimize nuisance tripping of the system, as defined here by the blowing of a fuse outside of the failure case, while keeping the both the reliable detection and the fast-acting times. In some applications such as extruder systems where an unexpected shutdown of the drive can lead to material solidification or compressor applications where a mid-stream shutdown leads to the shutdown of the whole process the costs of an erroneous shutdown are extremely high and the elimination of nuisance tripping become the critical consideration. Often the protection action requirements and the elimination of nuisance tripping are conflicting objectives, especially in drive systems that are installed in harsh environments where short term overload cycles and incoming voltage sags are common; once sufficient leeway is given to the fuse rating to allow overload cycles during under voltage conditions without the possibility of nuisance tripping – also allowing for normal aging of the fuse – the system might not react quickly enough to diode failures. Furthermore, these challenges are enhanced as the VA rating of the fuse increase. For 3.3 kV and 4.16 kV motor drive systems in square torque applications without demanding load cycles fuses can be reliable solution up to shaft powers of around 3 MW. However, as the application moves outside of this operational area the selection of cost-effective and reliable fused solutions becomes increasingly difficult.

Special care should be taken to reliably detect the failure of a diode. In general detection of a failure on the primary side of a 12-pulse rectifier transformer is problematic. Due to the phase shifting and local saturation of the transformer the primary side currents might not contain enough information to quickly and reliably recognize a diode failure. This is even more difficult for 18- and 24-pulse rectifier circuits. For this reason, most state of the art protection circuits are located on the secondary, i.e. drive side, of the transformer. Failures of diodes during normal operation and while active power is transferred through the rectifier system are easier to detect. This can be done by for example measuring the potential between the NP voltage of 3-level voltage source drives and the mid-point of a 12-pulse rectifier system. However, this mechanism will not function reliably when little or no power is transferred, for example in the stand-by case. Furthermore, the system should also be able to recognize when a circuit with a failed diode is being energized by the closing of an upstream circuit breaker. In this case the active power delivered by the drive system is negligible although significant reactive power flows can occur, especially if the main transformer is not pre-magnetized.

The identification sensitivity can be improved markedly by analysis of either the currents between the rectifier and the transformer or the voltages at the rectified ac terminals. Of the two options the voltage signal analysis is more robust and significantly less expensive, especially at high power levels. It should also be noted that the current signal contains large amounts of harmonic content in normal operation making identification more difficult. As example in [14] a method is described that monitors the voltages and detects the failure of a diode to block voltage reliably and very quickly. Allowing for typical commutation delays and transformer leakage impedances a detection of a failed diode is possible within 3 ms. As such this is much faster than any detection based on current since in this time period the current has not had enough time to build up to abnormal fault levels.

Once the fault is detected, as a next and final step the effects of the fault should be minimized. This should eventually take the form of isolating the circuit by opening a circuit breaker. However, circuit breakers will only truly open once the current crosses the zero point and, especially at medium voltage levels, require a significant opening time due to the physical mass that must be moved. In general circuit breakers require between 2 and 3 cycles to fully open and isolate the circuit. Therefore, even assuming that the fault is identified early enough, and the opening command is sent almost instantaneously, the full asymmetrical fault current had been flowing and the associated damage to transformer had already occurred at the point where the circuit breaker opens.

A reliable and sufficiently fast acting option is to create a symmetrical three phase short circuit on each of the transformer secondaries a soon as the diode fault is detected. In this case, with a detection of a fault occurs within 3 ms and the symmetric short circuit is initiated immediately, the single diode fault will be virtually indistinguishable from a bolted 3 phase short circuit from the transformer's point of view. This protection action can be achieved by installing fast short circuiting (earthing) devices directly on the ac terminals. However, these devices are typically single use and quite expensive. Another, more favorable, method is to directly short circuit the drive dc-link. This method also has the additional benefit that any associated arcing in the converter or cables is also extinguished.

VII. CONCLUSIONS

When a semiconductor fails in a rectifier system and starts to conduct to the reverse direction, it causes a short-circuit directly at the terminals of the transformer in the immediate vicinity of the failing converter. In this technical paper the diode reverse breakdown phenomenon called 'arc-back' has been clarified. There has not been design parameters available for the arc-back previously in the literature, only the theoretical value "3" has been available. The report concentrates on diode failures, the factors for controlled semiconductors are smaller in case the control circuit is intact.

In this paper, the theoretical value has been confirmed via simulations, as well saturation and the effect of the relation *X/R* in the phenomenon have been clarified. Also harmonic current components and RMS values have been clarified. From the simulated curves, the dynamic peak and thermal RMS values of arc-back are compared to each other as well to three-phase short-circuit.

According to the results, the diode failure causes higher dynamic currents and stresses as well higher thermal currents and stresses than a three-phase or single-phase short-circuit. The actual values are not as high as the theoretical value but the difference to the generally recognized three- and single-phase short-circuits is remarkable. In addition, forces are proportional to the square of the currents.

In order to avoid unwanted expensive transformer failures in the fuseless semiconductor systems, the diode failure detection or the transformer design has to be applied accordingly. The protection has to be reliable: the faults have to be detected but, at the same time, false alarms are undesirable. In this paper, different detecting options have been discussed. Once a diode fault has been detected the system has to be protected. One beneficial method is to directly short circuit the drive dc-link. The way to avoid the transformer failure has to be decided together with the customer due to the higher cost of the transformer or the detection system.

The arc-back fault needs to be taken into account in transformer dimensioning and protect. Thus this causes a need to update the transformer standards for VSDs, there the arc-back fault factor needs to be taken into account for dimensioning the transformer.

VIII. ACKNOWLEDGMENT

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